WHAT IS CLAIMED IS:

1. A process for forming a conductive via in an integrated circuit structure, where the integrated circuit structure includes a first dielectric layer overlying a first conductive layer, the process comprising:
   (a) forming a via cavity in the first dielectric layer, the via cavity exposing the first conductive layer;
   (b) etching the via cavity with a hydrogen-containing plasma;
   (c) forming a liner layer in the via cavity; and
   (d) forming a second conductive layer adjacent the liner layer in the via cavity, the second conductive layer substantially filling the via cavity to form the conductive via.

2. The process of claim 1 further comprising Argon sputtering the via cavity after step (b) and before step (c) to at least partially remove residue on the first conductive layer in the via cavity.

3. The process of claim 1 wherein step (b) further comprises stripping carbon and oxygen from a residue on the first conductive layer in the via cavity.

4. The process of claim 1 wherein step (b) further comprises forming hydrogen ions from at least one of the gases including N_2H_2, NH_3, and H_2.

5. The process of claim 1 wherein step (c) further comprises forming the liner layer by chemical vapor deposition of titanium nitride.

6. The process of claim 5 further comprising exposing the liner layer to an isotropic plasma of hydrogen and nitrogen ions after step (c) and before step (d), thereby densifying the liner layer prior to formation of the second metal layer.

7. The process of claim 6 further comprising forming the isotropic plasma by microwave excitation of at least one of the combinations of gases including N_2H_2, NH_3 and N_2, and H_2.

8. The process of claim 1 further comprising forming a titanium layer over and adjacent the first conductive layer in the via cavity after step (a) and before step (b).

9. The process of claim 1 wherein step (d) further comprises forming the second conductive layer of tungsten.

10. A process for forming a conductive via in an integrated circuit structure, where the integrated circuit structure includes a first dielectric layer overlying a first conductive layer, the process comprising:

(a) forming a via cavity in the first dielectric layer, the via cavity exposing the first conductive layer;

(b) forming a titanium layer over and adjacent the first conductive layer in the via cavity;

(c) etching the via cavity with a hydrogen-containing plasma, thereby stripping carbon and oxygen from a residue on the first conductive layer in the via cavity;

(d) Argon sputtering the via cavity to at least partially remove the residue on the first conductive layer in the via cavity;

(e) forming a titanium nitride liner layer in the via cavity;

(f) exposing the titanium nitride liner layer to an isotropic plasma containing hydrogen ions, thereby densifying the titanium nitride liner layer; and

(g) forming a tungsten layer adjacent the titanium nitride liner layer in the via cavity, the tungsten layer substantially filling the via cavity to form the conductive via.

11. A process for forming a conductive via in an integrated circuit structure, where the integrated circuit structure includes a first dielectric layer overlying a first conductive layer, the process comprising:

(a) forming a via cavity in the first dielectric layer, the via cavity exposing the first conductive layer;

(b) forming a liner layer in the via cavity;

(c) exposing the liner layer to an isotropic plasma containing hydrogen ions, thereby densifying the liner layer; and

(d) forming a second conductive layer adjacent the liner layer in the via cavity, the second conductive layer substantially filling the via cavity to form the conductive via.

12. The process of claim 11 wherein step (c) further comprises forming the isotropic plasma by microwave excitation of at least one of the combination of gases including N_2H_2, NH_3 and N_2, and H_2.

13. The process of claim 11 further comprising forming a titanium layer over and adjacent the first conductive layer in the via cavity after step (a) and before step (b).

14. The process of claim 11 wherein step (d) further comprises forming the second conductive layer of tungsten.

15. The process of claim 11 further comprising etching the via cavity with a hydrogen-containing plasma after step (a) and before step (b) to at least partially remove residue on the first conductive layer in the via cavity.

16. The process of claim 11 further comprising Argon sputtering the via cavity after step (a) and before step (b) to at least partially remove residue on the first conductive layer in the via cavity.

17. The process of claim 11 further comprising etching the via cavity with a hydrogen-containing plasma after step (a) and before step (b) to at least partially strip carbon and oxygen from a residue on the first conductive layer in the via cavity.

18. The process of claim 11 further comprising etching the via cavity with a hydrogen-containing plasma after step (a) and before step (b), where the hydrogen is formed from at least one of the gases including N_2H_2, NH_3, and H_2.

19. The process of claim 11 wherein step (b) further comprises forming the liner layer of titanium nitride by chemical vapor deposition.

20. The process of claim 11 further comprising forming a titanium layer over and adjacent the first conductive layer in the via cavity after step (a) and before step (b).